APPLICATION NOTES

QUARTZ CRYSTALS

The following considerations must be well studied in order to select the right crystal for your applications:

1) ASIC CHARACTERISTICS:

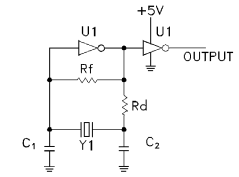
- Negative resistance.
- Small-signal gain analysis.
- Input and output resistance.
- Propagation delay between input and output of inverter.
- Gain-phase analysis.
- Supply voltage operational margin.
- Circuit configuration.
- Feedback resistor value (if integrated within the ASIC).
- Built-in load capacitance on X1 and X2 ports.
- Sensitivity of inverter operation versus stray inductance or capacitance due to layout or attachment methods.

2) CRYSTAL CHARACTERISTICS:

- Mode of Operation (Fundamental -vs.- Overtone).
- Series -vs.- Parallel.
- If Parallel: State “Load Capacitance”.
- If Overtone: specify design without inductor or conventional tuning tank LC Circuit.
- Maximum Resistance.
- Drive Level dependency.
- Operating Temperature.
- Frequency Accuracy at 25° C.
- Frequency Stability over Temperature.
- Aging.
- Pulling Characteristics.
- Spurious Responses.

3) CIRCUIT CONSIDERATIONS:

- **Select the best value for Rf (feedback resistor).** Recommend Value:
  Low kHz Range: between 10 MΩ to 20 MΩ
  MHz Range: between 100 kΩ to 1 MΩ
- **Select Series Resistance Value (Rd) for impedance matching.** Rd selection varies with ASIC negative resistance, output resistance and load impedance. Typical Value for Rd:
  0 Ω (Short) to 1 kΩ from 4 MHz to 30 MHz.
- **Study the Voltage Gain from output to input Vi / Vo = C2 / C1.** It is very common to select equal values of C1 and C2 in the circuit, but sometimes it is necessary to make the output load capacitance (C2) higher to compensate for the signal losses through the crystal and feed back loop.
- **Maximum Crystal Resistance Allowed.** Low resistance is desirable for better operational margin and stability. However, crystal resistance varies with frequency, blank size. Low crystal resistance could affect yield and therefore cost.
- **Typical Crystal Aging: ± 5 ppm per year maximum.** Aging over 10 years: ± 10 ppm to ± s15 ppm maximum. Tighter aging (up to ±1 ppm per year max.) is available. Tighter aging requires extremely high design, manufacturing and additional post-tests.
- **Inductorless Third (3rd) Overtone:** The Inductorless 3rd-Overtone circuit is similar to the fundamental frequency circuit except the feedback resistor value is made much smaller (typical value varies between 2 kΩ to 6 kΩ). In this case, the component of inductive admittance due to the resistor is greater than the admittance of the loading capacitance at the fundamental frequency, thereby preventing oscillation at the fundamental frequency. In the meantime, the inductive admittance at the overtone is less than the admittance of the Load Capacitor thus enabling the oscillation at the third-overtone. (See figure 1.)



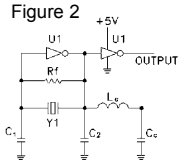
U1: ASIC
Y1: Crystal
C_1 C_2: Load Capacitance

Figure 1

Tuning Tank LC Overtone Circuit

- In an overtone mode, an additional inductor L1 and capacitance C_C is required to select the 3rd-Overtone mode, while suppressing or rejecting the fundamental mode. Choose L_C and C_C component values in the 3rd-overtone crystal circuit to satisfy the following conditions:
- The L_C / C_C component form a series resonant circuit at a frequency below the fundamental frequency, which makes the circuit look inductive at the fundamental frequency. This condition does not favor to oscillation at the fundamental mode.
- The L1 / C_C and C2 components form a parallel resonant circuit at a frequency about half-way between the fundamental and 3rd-Overtone frequency. This condition makes the circuit capacitive at the 3rd-Overtone frequency, which favors the oscillation at the desired Overtone mode. (See figure 2).

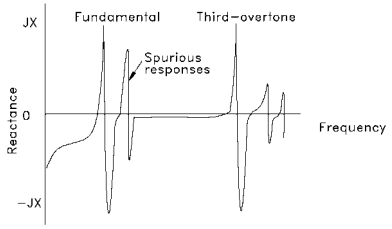
Figure 2



- The Lc tank may be located at either input or output of the inverter. However, the Lc tank at the out put is referred, because it helps to clean up all unwanted modes before signal goes through the crystal.

4) CONTROL UNWANTED MODES IN CRYSTALS:

Unwanted modes are resonant modes in addition to the desired modes (Fundamental, Third-Overtone, Fifth overtone, etc.). The frequencies of these unwanted modes are usually slightly higher than the desired modes within couple of hundreds kilohertz. In oscillator applications, it is necessary to control unwanted modes as lower as possible to prevent circuit oscillating in the "spurious mode". See Figure 3. The design of large electrodes on crystal to produce large pulling is a common cause of promoting spurs. Unwanted modes are usually specified in terms of resistance or in terms of the ratio of resistance of the unwanted mode to the resistance of the main mode over a bandwidth of desired frequency. A resistance ratio of 2:1 or a minimum of 3dB separation is usually adequate.



APPLICATION NOTES

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Q: Why does my crystal works sometimes, but not others?

A: This is the most common complaint heard from crystal users. Unless the crystal supplier knows this common mode of failure, and applies preventive measures, this common problem can be solved earlier in design stage. Some customers describe these crystals as "sleeping crystals". The circuit start-up sometimes and does not at other times, unless been touched with a scope probe or fingers. Abracon predicts this problem in our Design and Process Failure Mode Effect Analysis (DFMEA and PFMEA) with two main root causes:

a) Blank cleanliness.
b) Drive level dependency.
c) IC matching.

• Blank cleanliness: We use special blank wafer ultrasonic cleaning procedure in De-ionized water and 99.99% Isopropyl Alcohol with modulated air method to guarantee highest quality.

• Drive level dependency: On most production lots, we perform 100% DLD tests at five levels minimum starting from 1µW to 500µW. The DLD test will guarantee that the changes in ESR and frequency are within maximum limits thus assure the initial power start-up.

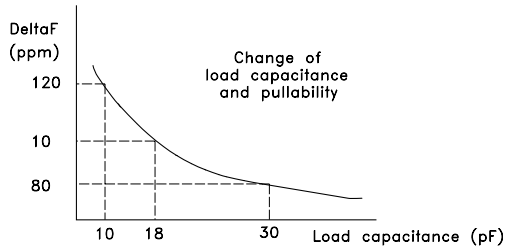
Typical ΔFDLD: ± 5ppm max.
Typical ΔRDLD: 25% max.

• IC matching: Abracon offers IC matching process to our customers in early design stage. The IC matching process will identify the optimum values of load capacitors, feedback and series resistors, drive level vs. load cap, voltage margin, open-loop gain at resonance, and temperature characteristics. Please consult Abracon for details.

Q: How to specify a pulling crystal?

A: Many applications in VCXO, PLL network require a crystal with pulling characteristics. The pullability of the crystal can be explained as follow:
When a crystal is operating at parallel resonance, it looks inductive in the circuit. As the reactance changes, the frequency changes correspondingly, thus change the pullability of the crystal. The difference between the Fs and Fa depends on the ratio C0/C1 ratio of the crystal.

The following crystal parameters specify the pullability:
• Motional capacitance C1 in fF.
• Motional inductance L1 in mH
• The difference of the parallel resonant frequency
ΔF = FL2 – FL1



• Ratio of shunt capacitance to motional capacitance C0/C1. The smaller ratio the better the pulling.

The pullability of the crystal can be designed to meet customer's requirements. However, the pulling function varies with package size, electrode size, frequency, load capacitance range, and operating mode. Please contact Abracon whenever you have a need for a pulling crystal.

Q: What is the trend of crystal packaging and advantages?

A:
• Minimizing the size and weight of mobile communication application such as cellular phones, PCMCIA, PDA, etc.
• Improve sealing technologies from resin sealing to seam sealing to Electron beam sealing.

• Advanced small quartz blank design in smaller ceramic packages such as 5.0 x 3.2mm, 3.2 x 2.5mm, etc. The fundamental frequency increases up to 66MHz helps simplify circuit design and is more efficient compared to the old traditional third-overtone circuit complexity.
• Features of E-Beam sealing:
✓ Tight stability and tight tolerance (±10ppm).
✓ Low ESR and high reliability by vacuum package.
✓ Resistance to shock and moisture.
✓ High productivity captured with seam sealing method.
✓ Miniaturization by fine processing of E-Beam.

• LTCC packaging helps reducing size and external components.

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